

# X-ray Microcalorimeter Arrays Fabricated by Surface Micromachining

G. C. Hilton<sup>a\*</sup>, J. A. Beall<sup>a</sup>, S. Deiker<sup>a</sup>, L. R. Vale<sup>a</sup>, W. B. Doriese<sup>a</sup>, Jörn Beyer<sup>b</sup>, J. N. Ullom<sup>a</sup>, C. D. Reintsema<sup>a</sup>, Y. Xu<sup>a</sup>, K. D. Irwin<sup>a</sup>

<sup>a</sup>National Institute of Standards and Technology, Boulder, CO, 80305 USA

<sup>b</sup>Physikalisch-Technische Bundesanstalt, Berlin D-10587 Germany

We are developing arrays of Mo/Cu TES-based detectors for use as x-ray microcalorimeters and sub-millimeter bolometers. We have fabricated  $8 \times 8$  pixel x-ray microcalorimeter arrays using surface micromachining. Surface-micromachining techniques hold the promise of scalability to much larger arrays and may allow for the integration of in-plane multiplexer elements. In this paper we describe the surface micromachining process and recent improvements in the device geometry that provide for increased mechanical strength. We also present x-ray and heat pulse spectra collected using these detectors.

## 1. INTRODUCTION

The excellent energy resolution of transition-edge sensor (TES) x-ray microcalorimeters [1, 2] and the compatibility of these sensors with SQUID multiplexing [3,4] make them promising candidates for array detectors at a variety of photon energies. Arrays are important not only for imaging applications such as those in astronomy, but for any application that would benefit from an increase in detector collection area such as x-ray microanalysis.

Because these detectors operate by sensing a temperature change from the absorption of incident radiation, they require a thermal isolation structure that both limits the thermal conductance to the pixel and provides mechanical support for the pixel. In most of the TES devices reported to date, the thermal isolation structure consists of a low stress  $\text{Si}_3\text{N}_4$  membrane. The membrane is formed by first depositing the nitride film on the front surface of the wafer and then removing the Si substrate from beneath the pixel. In some cases, the membrane is then perforated to further reduce the thermal conduction.

Single-pixel TES detectors are often fabricated

using a heated KOH solution to etch the substrate from beneath the pixel. While this method works well, it is difficult to make arbitrary patterns because this anisotropic etch only removes material from certain crystalline planes. Moreover, it is impossible to make a square pixel with vertical sidewalls, the preferred geometry for a close-packed pixel array.

It is also possible to etch the Si underneath the pixel using deep-reactive ion etching (DRIE). With DRIE it is possible to etch an arbitrary pattern with vertical sidewalls underneath the pixel. A key feature of detector arrays fabricated by DRIE or other bulk micromachining methods is the support grid of Si that remains in the inter-pixel spaces. The desire for mechanical strength, inter-pixel wiring area, and good thermal conduction drive the design toward a thick-walled grid, while array filling-factor requirements favor a thin-walled grid. For some applications it may be difficult to meet these competing requirements.

An alternative method for building arrays of thermal isolation structures is surface micromachining. Here a sacrificial layer is deposited and patterned on a Si substrate. This is followed by the deposition of the membrane material. The sacrificial layer is then removed leaving a low-thermal-conduction membrane supported above

---

\*Corresponding author. email hilton@boulder.nist.gov. This work is supported in part by funding from the NASA Cross-Enterprise program. Contribution of NIST, not subject to copyright

the substrate. This method has been used to make arrays of room-temperature thermal detectors [5,6]. Recently we have developed a process to fabricate TES detectors using surface micromachining [7]. Surface micromachining has many potential advantages over bulk micromachining for TES arrays. Because the substrate is left intact, handling of completed devices is greatly simplified. More importantly, nearly all of the under-pixel area is left open and may potentially be used for under-pixel wiring or in-plane multiplexing and readout circuitry.

## 2. FABRICATION AND RESULTS

The small pixel sizes used in room-temperature thermal detectors ( $\sim 20 \mu\text{m}$ ) allow a conventional plasma etch to be used to remove the sacrificial layer from underneath the detector membrane. These detectors are generally fabricated using polyimide as a sacrificial layer and low-temperature PECVD  $\text{Si}_3\text{N}_4$  as the membrane material. An oxygen plasma etch is then used as a sacrificial etch to remove the polyimide. In order to fabricate the much larger TES detector pixels ( $200 \mu\text{m} - 1 \text{ mm}$ ) a different etch procedure must be used. The lateral extent of a plasma etch is limited by wall interactions to a few times the thickness of the sacrificial layer. Wet etching of the sacrificial layer is possible, however diffusion of fresh etchant under the membrane is very slow, and critical-point drying techniques must be used to prevent surface tension from destroying the membrane.

We have developed a technique for fabricating surface micromachined detectors using a  $\text{XeF}_2$  plasma-less dry Si etch [8]. In our process [7] we first deposit the sacrificial layer ( $2 \mu\text{m}$  of LPCVD poly-Si) onto oxidized Si wafers and pattern it into pixel-sized islands. The membrane layer ( $500 \text{ nm}$  of LPCVD  $\text{Si}_3\text{N}_4$ ) is then deposited on the wafer. Fabrication of the Mo/Cu TES and Bi absorber are then carried out using our standard procedure [9]. Because of the large step height of the membrane over the sacrificial layer, we utilize an additional  $500 \text{ nm}$  thick Nb wiring layer. The detectors are then completed by opening access holes in the  $\text{Si}_3\text{N}_4$  membrane, and removing the

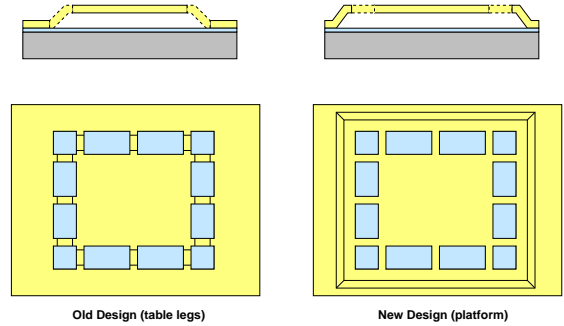


Figure 1. Schematic view of original and improved geometries for surface micromachined TES detector arrays.

underlying Si using the  $\text{XeF}_2$  etch.

In our initial fabrication runs we obtained very low yield. Many of the pixels (particularly those with Bi absorbers) would break as the pixels were cooled from room temperature to  $4\text{K}$ . This breakage can be attributed to the large difference in coefficient of thermal expansion between the metallic detector elements and the low thermal expansion membrane and substrate. As the device is cooled, the edges of the membrane are placed under tension by the metallic layers. This problem is exacerbated by our original pixel design shown schematically in Figure 1. In this design, the etch access holes were placed so that they overlapped with the edge of the sacrificial layer. When the sacrificial layer is removed, the remaining membrane resembles a table surrounded by many short vertical legs. We have since modified the positioning of the access holes to be roughly  $5 \mu\text{m}$  inside the edge of the sacrificial layer. The membrane now resembles a platform with in-plane perforations with a solid membrane “collar” surrounding the step edge. Because the forces applied at the perforations are now all in-plane, this membrane is much stronger and we obtain near 100 % yield. Photographs of completed devices are shown in Figures 2 and 3.

We have measured several chips containing 64 pixels using both multiplexed and single channel readout and have illuminated two chips with x-rays from an  $^{55}\text{Fe}$  radioactive source. The chips measured thus far do not have Bi absorbers. The measured chips had a superconducting transition

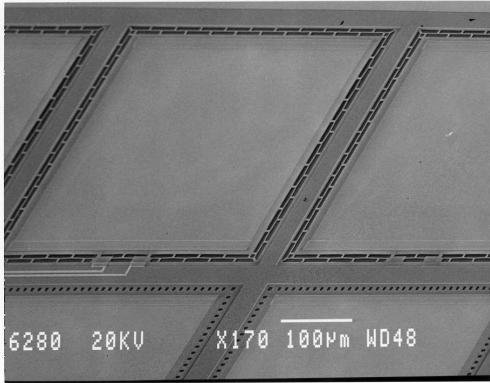


Figure 2. Scanning electron micrograph showing two pixel thermal designs, a low thermal conductance design (upper pixels) and a high thermal conductance design (lower pixels).

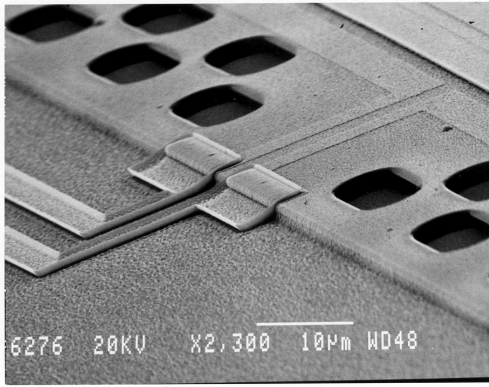


Figure 3. Scanning electron micrograph showing the details of the Nb wiring layer and the edge of the membrane and perforations in the membrane.

temperature ( $T_c$ ) of 95-102 mK, and a normal state TES resistance of roughly 17 m $\Omega$ . Because each array contained several different perforation designs the thermal conductance and bias powers varied from pixel to pixel. Heat-pulse and x-ray spectrum obtained are shown in Figure 4. We believe the broadening of the heat pulses is due to x-rays that are absorbed under the pixel because of the lack of a highly attenuating absorber. The broadening of the x-ray spectra is due to both these substrate hits and some positional dependence. Similar data has been obtained using multiplexed readout on an uncollimated array. [10]

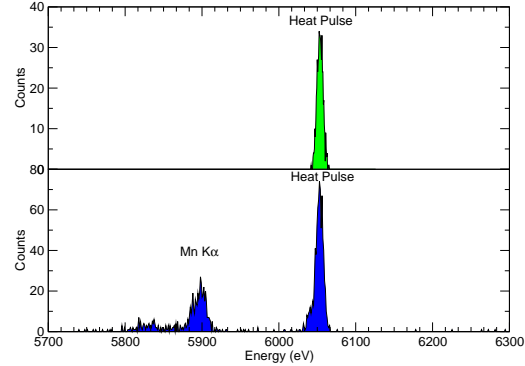


Figure 4. Heat-pulse (upper) and x-ray spectrum for Mn  $K_\alpha$  x-rays with collimation (lower). The measured resolution for heat pulses with no incident x-ray is 10 eV. When x-ray are applied the heat-pulse resolution broadens to 13 eV and develops a low energy tail. The energy resolution for Mn  $K_\alpha$  x-rays is 22 eV.

The authors acknowledge Marcel van den Berg for expert assistance with analysis software.

## REFERENCES

1. K. D. Irwin *et. al*, Nucl. Instr. Meth. A444 (2000) 184–187.
2. W. M. B. Tiest *et. al*, Low Temperature Detectors, American Institute of Physics, 2001, pp. 199–202.
3. J. A. Chervenak *et. al*, Appl. Phys. Lett. 74 (26) (1999) 4043–5.
4. K. D. Irwin, PHYSICA C 368 (1-4) (2002) 203 – 210.
5. P. Eriksson *et. al*, Journal of Microelectromechanical Systems 6 (1) (1997) 55–61.
6. B. Cole *et. al*, PROCEEDINGS OF THE IEEE 86 (8) (1998) 1679 – 1686.
7. G. C. Hilton *et. al*, IEEE Trans. Appl. Supercond. in press .
8. F. I. Chang *et. al*, Proc. SPIE 2641 (1995) 117–128.
9. G. C. Hilton *et. al*, IEEE Transactions on Applied Superconductivity 11 (1) (2001) 739–742.
10. W. Doriese *et. al*, These proceedings.